010327-007410US George B. F. Yee, Reg. No. 37,478 Telephone: 650-326-2400 Inventor: John Marino Title: Hardware Implementation of an N-Way Dynamic Linked

+

Sheets of drawings 1 of 10

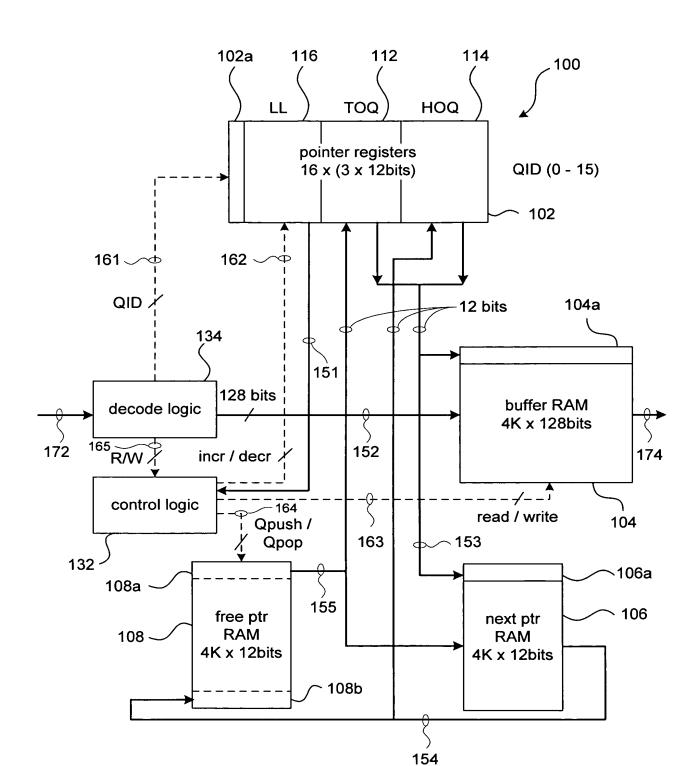
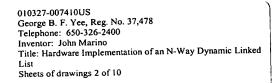


Fig. 1



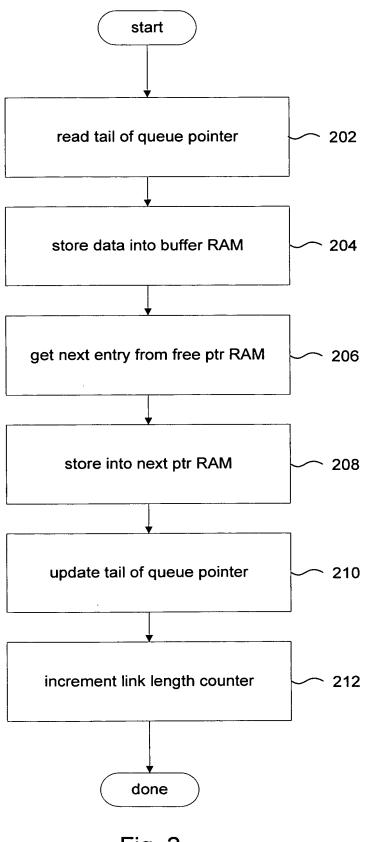


Fig. 2 (write)

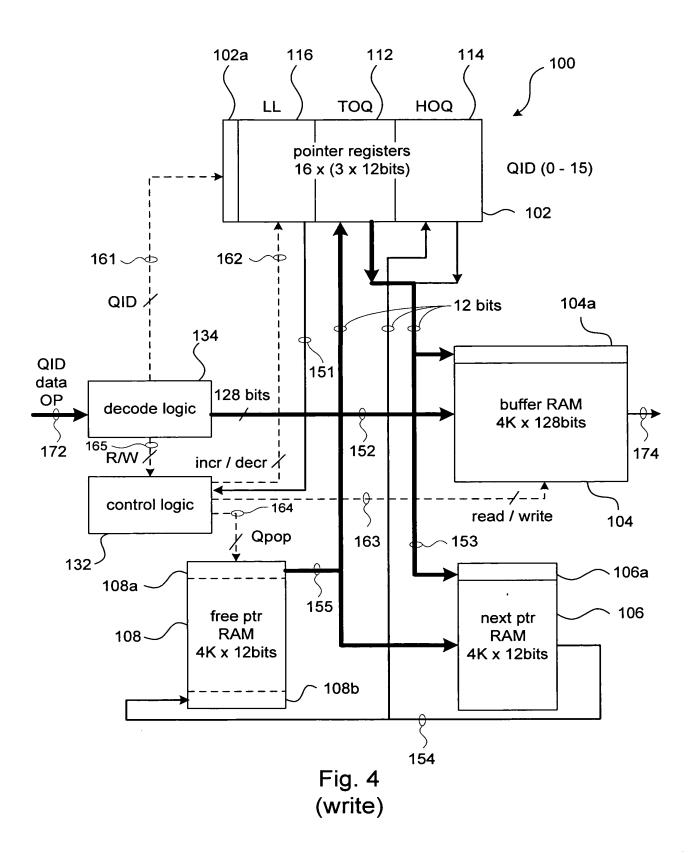
010327-007410US
George B. F. Yee, Reg. No. 37,478
Telephone: 650-326-2400
Inventor: John Marino
Title: Hardware Implementation of an N-Way Dynamic Linked
List
Sheets of drawings 3 of 10

202 Tail Tail data 204 **Buffer RAM** 108a ➤ NextValid 206 FreePtr RAM Tail NextValid 208 NextPtr RAM NextValid Tail Fig. 3

010327-007410US
George B. F. Yee, Reg. No. 37,478
Telephone: 650-326-2400
Inventor: John Marino
Title: Hardware Implementation of an N-Way Dynamic Linked

+

Sheets of drawings 4 of 10



010327-007410US
George B. F. Yee, Reg. No. 37,478
Telephone: 650-326-2400
Inventor: John Marino
Title: Hardware Implementation of an N-Way Dynamic Linked
List
Sheets of drawings 5 of 10

+

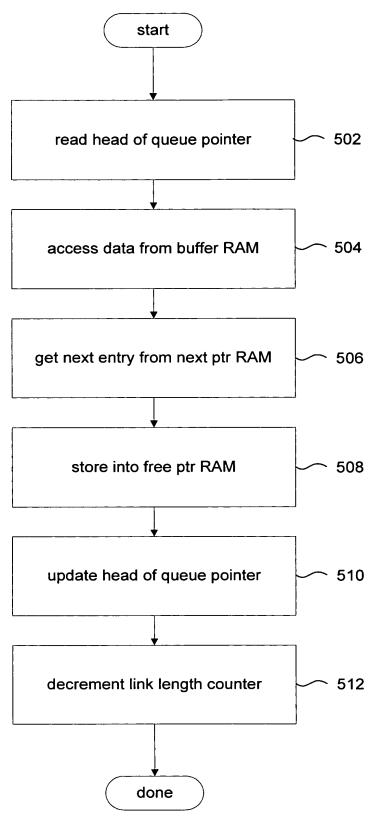
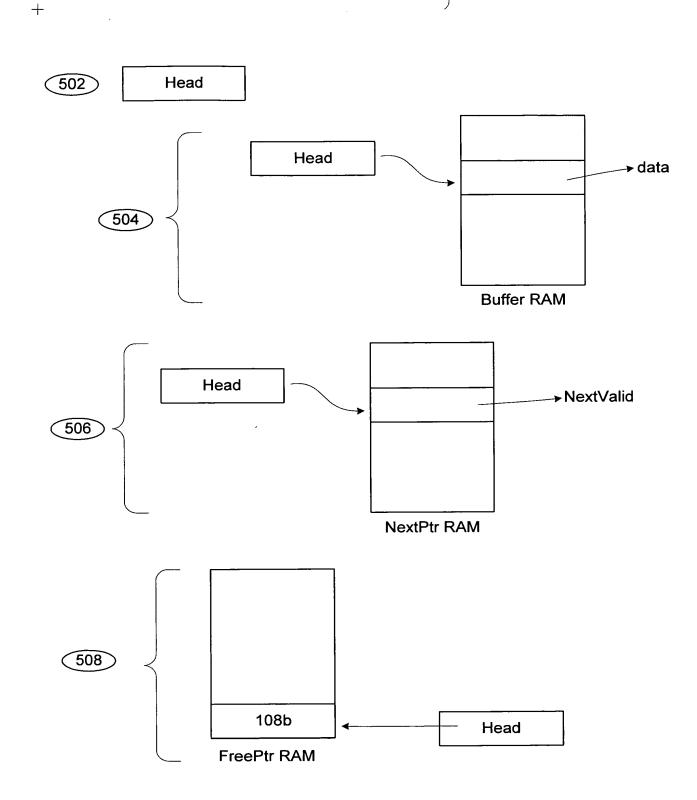
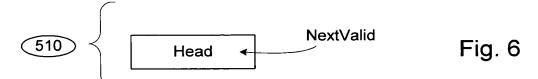


Fig. 5 (read)

010327-007410US George B. F. Yee, Reg. No. 37,478 Telephone: 650-326-2400 Inventor: John Marino Title: Hardware Implementation of an N-Way Dynamic Linked

Sheets of drawings 6 of 10





010327-007410US

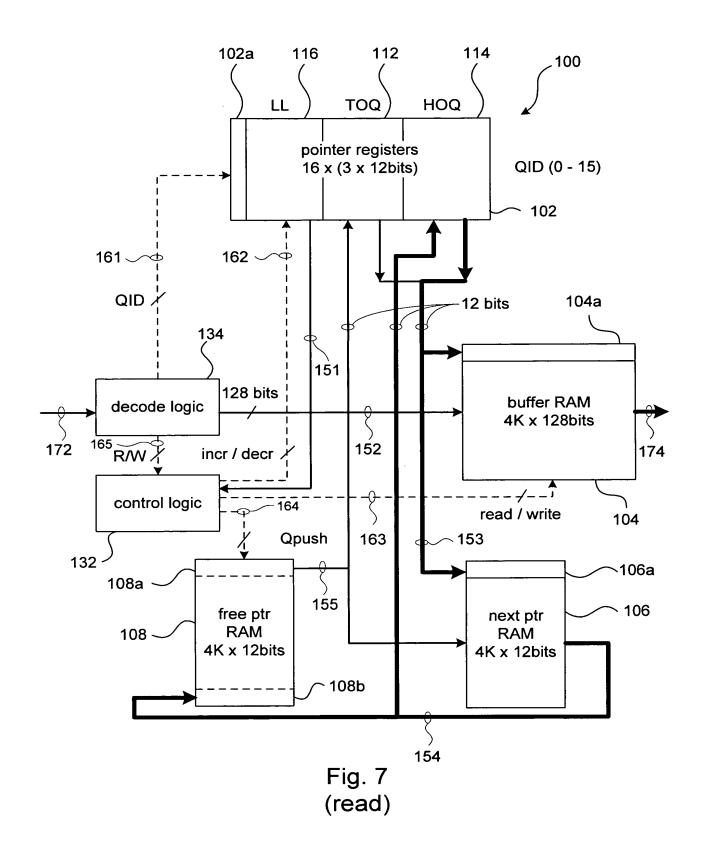
George B. F. Yee, Reg. No. 37,478 Telephone: 650-326-2400

Inventor: John Marino

Title: Hardware Implementation of an N-Way Dynamic Linked List

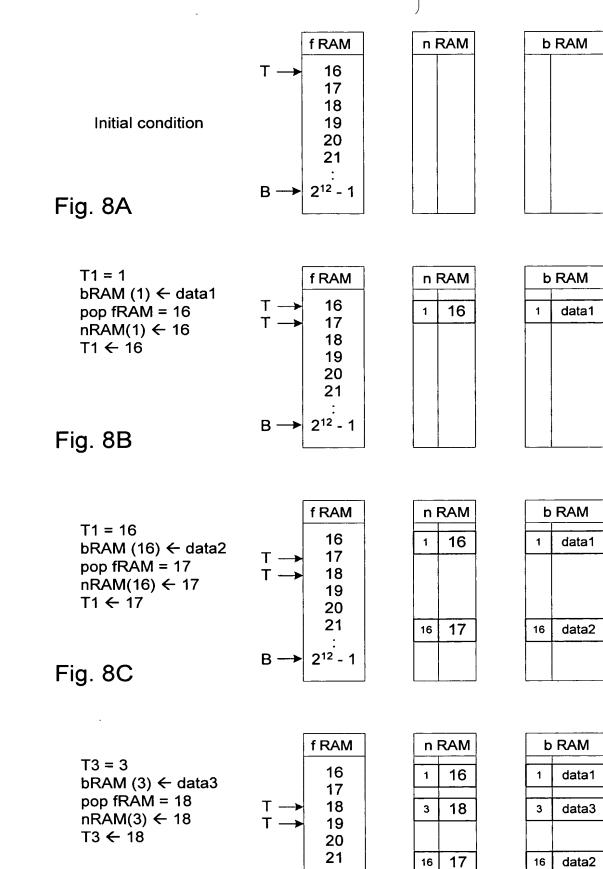
+

Sheets of drawings 7 of 10



010327-007410US
George B. F. Yee, Reg. No. 37,478
Telephone: 650-326-2400
Inventor: John Marino
Title: Hardware Implementation of an N-Way Dynamic Linked
List
Sheets of drawings 8 of 10

+



 $2^{12} - 1$

Fig. 8D

+

010327-007410US George B. F. Yee, Reg. No. 37,478 Telephone: 650-326-2400 Inventor: John Marino

Title: Hardware Implementation of an N-Way Dynamic Linked

f RAM

16

17

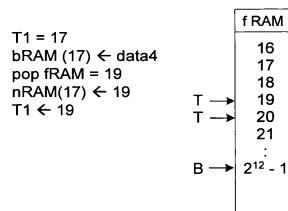
18

19

20 21

+

Sheets of drawings 9 of 10

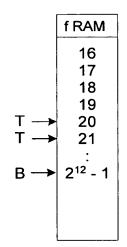


n	RAM			
1 16				
3	18			
16	17			
17	19			

	b	RAM
	1	data1
Ì		
	3	data3
	16	data2
	17	data4

T3 = 18bRAM (18) ← data5 pop fRAM = 20nRAM(18) ← 20 T3 ← 20

Fig. 8E



n	RAM
1	16
3	18
16	17
17	19
18	20

b RAM			
1	data1		
3	data3		
16	data2		
17	data4		
18	data5		

H1 = 1bRAM(1) = data1nRAM(1) = 16fRAM ← H1 (push) H1 ← 16

n	RAM
1	16
3	18
16	17
17	19
18	20

b RAM			
	_		
1	_data1		
3	data3		
16	data2		
17	data4		
18	data5		

Fig. 8G

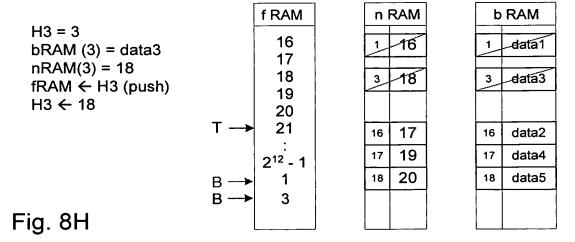
Fig. 8F

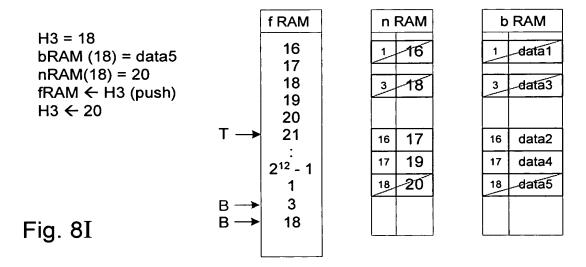
010327-007410US George B. F. Yee, Reg. No. 37,478 Telephone: 650-326-2400

Inventor: John Marino Title: Hardware Implementation of an N-Way Dynamic Linked

+

Sheets of drawings 10 of 10





T1 = 19 bRAM (19) ← data6 pop fRAM = 21 nRAM(19) ← 21 T1 ← 21		f RAM	n RAM		b
		16 17 18 19 20	1 16		3
	T → T →	20 21 22 :	16 17 17 19	-	16 17
		2 ¹² - 1	18 20 19 21	<u> </u> -	18
Fig. 8J	В →	3 18	13 21		

b RAM

data1

data3

data2

data4 data5

data6